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(71) Applicant: **STMicroelectronics S.r.l.**
20041 Agrate Brianza (Milano) (IT)

(72) Inventor: **Ravesi, Sebastiano**
95030 Sant'Agata li Battiati (Catania) (IT)

(74) Representative: **Botti, Mario**
Botti & Ferrari S.r.l.
Via Locatelli, 5
20124 Milano (IT)

(54) **Method for manufacturing capacitor elements on a semiconductor substrate**

(57) A method for manufacturing integrated capacitive elements (C) on a semiconductor substrate (1), comprising at least the steps of:

- forming a first dielectric layer (2) over said semiconductor substrate (1);
- depositing a first metallization layer (3) on said first dielectric layer (2);
- defining said first metallization layer (3) to provide lower plates (4) of capacitive elements and interconnection pads (5) in said dielectric layer (2);
- forming a second dielectric layer (6) over said first dielectric layer;
- forming first openings (7) aligned with said lower plates through said second dielectric layer;
- depositing a third dielectric layer (8) on said first dielectric layer and inside said first openings (7);
- forming second openings (9) through said third dielectric layer aligned with said interconnection pads (5);
- depositing a fourth dielectric layer (10) on the whole wafer surface, said fourth dielectric layer (10) being "etchable" in a completely selective manner relative to said third dielectric layer (8);
- forming third openings (11) through said fourth dielectric layer aligned with said lower plates (4) as far down as the third dielectric layer (8);
- forming fourth openings (12) through said fourth dielectric layer (10), and the second dielectric layer (6) beneath, aligned with the second openings as far down as said pads (5);
- depositing a second metallization layer (13) and in said third (11) and fourth (12) openings, to respectively provide upper plates (13) for the capacitive elements (C) and complete interconnections (14) to the interconnection pads (5).

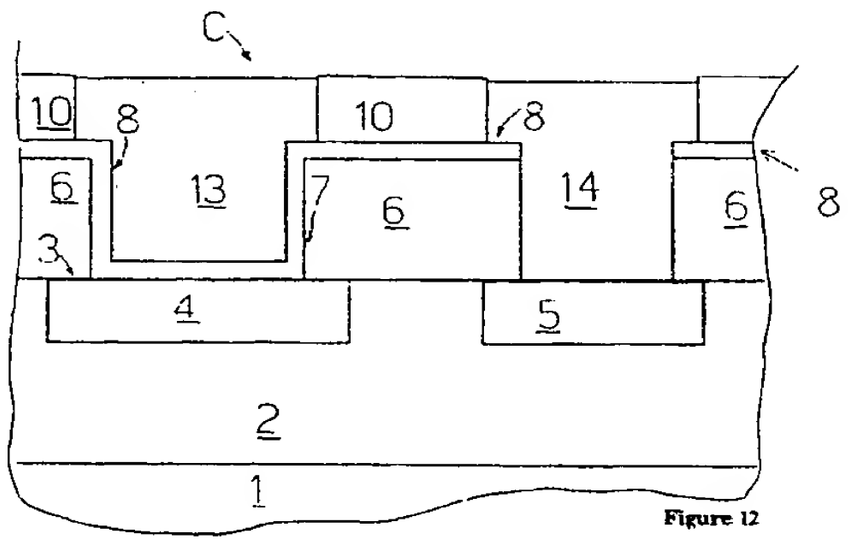

Figure 12

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Description

Field of the Invention

[0001] This invention relates to a method for manufacturing integrated capacitive elements on a semiconductor substrate.

[0002] The invention specifically relates to a method for manufacturing capacitive elements on a semiconductor substrate, comprising at least the steps of:

- forming a first dielectric layer over said semiconductor substrate;
- depositing a first metallization layer on said first dielectric layer;
- defining said first metallization layer to provide lower plates of capacitive elements and interconnection pads in said dielectric layer;
- forming a second dielectric layer over said first dielectric layer.

[0003] The invention particularly, but not exclusively, relates to a method for manufacturing capacitive elements of high capacitance which are interposed between successive metallization levels within a multi-level connection structure, implementing in particular a so-called "dual damascene" interconnection scheme, and the description which follows will make reference to such a field of application for simplicity of illustration.

Prior Art

[0004] As is well known, capacitive elements are passive components diffusely employed in integrated electronic circuits.

[0005] A known technique for integrating metal plate capacitors on a semiconductor substrate comprises the formation, after an oxide layer has been formed on the semiconductor substrate, of a metallization layer over the oxide layer. The metallization layer is patterned to provide the lower plates of the capacitive elements and any interconnection pads.

[0006] A thin lower dielectric layer is then deposited over the entire exposed surface and intended to provide the dielectric layer separating the plates of the capacitive elements.

[0007] Those portions of the lower dielectric layer which overlie the metallization pads are removed by a photolithographic process, to later allow of the interconnection of such pads to the next metallization layer.

[0008] An upper dielectric layer is then deposited over the entire wafer surface.

[0009] Subsequently, openings are formed through this dielectric layer aligned with the metallization pads and the lower dielectric layer overlying the lower plates.

[0010] The upper dielectric layer has to be etchable in a completely selective manner relative to the lower dielectric layer.

[0011] Were not the upper dielectric layer etchable relative to the lower dielectric layer, the lower dielectric layer might be destroyed or damaged during the formation of the contact openings, thereby compromising the operability of the capacitive elements.

[0012] The manufacturing of the capacitive elements is completed by the deposition and subsequent photolithographic definition of the next metallization level.

[0013] The last-mentioned step defines the upper plates of the capacitive elements and the interconnection to the lower metallization level through the openings.

[0014] Although in many ways advantageous, the above manufacturing method comprises depositing an oxide layer which is used to provide the dielectric layer between the plates of the capacitive elements and must have adequate characteristics to ensure functional capacitors, so that it must be suitably provided and realized in standard manufacturing schemes.

[0015] The underlying technical problem of this invention is to provide a method for manufacturing capacitive elements, in particular high-capacitance capacitors having such structural and functional features as to be integratable to processes for manufacturing semiconductor-integrated electronic devices without modifying the various steps of the manufacturing process, thereby overcoming the drawbacks of prior art processes for manufacturing capacitive elements.

Summary of the invention

[0016] The concept behind this invention is one of producing the aforementioned integrated capacitive elements by the very steps of a conventional process for forming interconnections in integrated circuits, in particular a process known as "dual damascene". More particularly, the method of this invention provides two layers of an insulating material distinguishable from each other during the removing and etching steps carried out within the multi-level interconnection scheme.

[0017] Based on this concept, the technical problem is solved by a method as described in the characterizing portion of Claim 1.

Brief Description of the Drawings

[0018] In the drawings:

Figures 1-4 are vertical cross-sectional views showing schematically a portion of a semiconductor substrate wherein an interconnection structure has been formed according to the prior art;

Figures 5-12 are vertical cross-sectional views showing schematically a portion of a semiconductor

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substrate whereto the steps of the method for manufacturing capacitive elements according to the invention have been applied.

Description of the Invention

[0019] Referring to Figures 1 to 4, an interconnection scheme known as "dual damascene", which is currently used to provide interconnections in integrated circuits, will be described first.

[0020] A first dielectric layer 20 is formed over a semiconductor substrate 100. A metallization layer 30 is then formed over the dielectric layer 20 and patterned to provide a plurality of plates or pads 40 in the first dielectric layer 20.

[0021] A second dielectric layer 50, and a third dielectric layer 60 known as the etch stop layer, are then deposited successively as shown in Figure 1.

[0022] Using a conventional photolithographic process, a first opening 70 is formed through the dielectric layer 60 aligned with the underlying pad 40 which will serve for interconnecting the successive metallization layers.

[0023] As shown in Figure 3, a fourth dielectric layer 80, identical with the second dielectric layer 50, is then deposited.

[0024] A second opening 90 (Figure 4) is then formed by a single masking step whereby larger openings 110 are defined than the openings 70.

[0025] During the etching operation for forming the second openings 90, the fourth dielectric layer 80 is first removed. Thereafter, utilizing the complete selectivity of this etch relative to the third dielectric layer 60, the etching is continued through the second dielectric layer 50 and stopped at the surface of the underlying pad 40.

[0026] A second metallization layer 120 is then deposited to provide the interconnection (Figure 5) to the pad 40 through the openings 130.

[0027] This metallization layer 120 is then subjected to an etchback or CMP (Chemical Mechanical Polishing) step to locate it within the overall dielectric layer comprised of the second, third and fourth dielectric layer.

[0028] The above process flow is used to implement a multi-level interconnection scheme.

[0029] Advantageously, a method for manufacturing capacitive elements C integrated on a semiconductor substrate 1 which comprises, in accordance with the invention, the previously described process steps for providing interconnections will now be described.

[0030] The method steps and the structures described hereinafter form no complete integrated circuit manufacturing method. The invention can be practiced along with the integrated circuit manufacturing techniques currently in use by the industry, and only such commonly used process steps as are necessary to an understanding of this invention will be discussed.

[0031] The drawing figures that show cross-sections through portions of an integrated circuit during its manufacturing process are not drawn to scale, but rather to highlight major features of the invention.

[0032] A first dielectric layer 2 is formed on a semiconductor substrate 1.

[0033] The total thickness of this first dielectric layer 2 is the sum of the individual thickness of the silicon oxide layers, which have been grown by the various thermal oxidation operations carried out during the manufacturing of the elementary devices used in standard integrated circuits, and those of the dielectrics comprising between successive metallization levels.

[0034] Advantageously, the larger the thickness of this first total dielectric layer 2, the smaller becomes its dielectric permittivity and the higher the ratio of the capacitor C, as provided by the inventive method, own capacitance to the parasitic capacitance toward the substrate.

[0035] Using conventional manufacturing steps, a plurality of plates 4 are defined in this first dielectric layer 2 which will function as the lower plate of the capacitor, as well as a plurality of interconnection pads 5 which will be used for interconnecting device or functional blocks provided in the integrated circuit to the connection to the next metallization layer 1.

[0036] Advantageously, the plates 4 and pads 5 are formed in the same first metallization layer 3.

[0037] In particular, this first metallization layer 3 could belong to an intermediate metallization layer, and is not required to be the first metallization layer formed in the integrated circuit.

[0038] Once the plates 4 and pads 5 are formed, a second dielectric layer 6 is deposited.

[0039] The next manufacturing step comprises the formation of first openings 7 through the second dielectric layer 6 only aligned with the plates 4 which will be used as the lower plate of a capacitor that will be formed, as shown in Figure 7.

[0040] From this step onwards, the method steps follow a standard scheme with standard dual damascene processes. That is, a third dielectric layer 8, known as the etch stop layer, is deposited on top of the second dielectric layer 6, as shown in Figure 8.

[0041] This third dielectric layer 8 has, in the method of this invention, an important dielectric function for the capacitive element C.

[0042] Advantageously, this third dielectric layer 8 can be deposited using reduced thermal budget processes which are compatible with the underlying metal films. This third dielectric layer 8 has good adherence on metal and high electric permittivity, thereby allowing capacitors C of high specific capacitance that will be manufactured. In addition, this third dielectric layer 8 is made from high dielectric strength materials.

[0043] The thickness of the third dielectric layer 8 should be adequate to ensure a higher specific capacitance, and therefore, should be the thinnest, but sufficiently strong not to impair functionality in the course of

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subsequent method steps to be applied thereto.

[0044] The third dielectric layer 8 should be deposited to a conforming, i.e. even, thickness, even at the edge of the lower plate 4 of the capacitor that has been defined by the previous method providing the openings 7 through the second dielectric layer 6.

[0045] Advantageously, this third dielectric layer 8 is formed from materials of high dielectric permittivity, such as tantalium or titanium oxide and strontium and barium/strontium titanates, to be obtained by chemical vapor deposition from metal-organic precursors.

[0046] As shown in Figure 9, the next method step comprises forming second openings 9 by conventional etching through this third dielectric layer 8.

[0047] These second openings 9 are provided aligned with the underlying pad 5 whereby the interconnection to the next metallization layer will be established.

[0048] A fourth dielectric layer 10 is then deposited over the entire wafer surface.

[0049] Advantageously, this fourth dielectric layer 10 is formed from a material which can remove or attenuate the presence of steps at the wafer surface, is compatible in the process with the underlying structure, and has good adherence on the layer beneath.

[0050] Furthermore, this fourth dielectric layer 10 is "etchable" in a completely selective manner in the respect of the third dielectric layer 8 as provided for by the dual damascene scheme.

[0051] The next manufacturing step comprises forming third openings 11 through the fourth dielectric layer 6 aligned with the plates 4 which will be used as the lower plate of a capacitor that will be formed, and fourth openings 12 through the fourth dielectric layer 6 aligned with the second openings 9, as shown in Figure 11.

[0052] Advantageously, these fourth openings 12 are larger than said second openings 9.

[0053] Advantageously, by utilizing the complete selectivity of the fourth dielectric layer 10 with the third dielectric layer 8, and where the second dielectric layer 6 is made from the same material as the fourth dielectric layer 10, the etching of the fourth dielectric layer 10 is continued through the second dielectric layer, and the fourth openings 12 reach the pads 5.

[0054] The manufacturing of the capacitors C is completed by the deposition and definition of a second metallization layer 12 by an etchback or CMP step, as shown in Figure 12.

[0055] The last-mentioned method step defines an upper plate 14 of the capacitor C and an interconnection to the first metallization layer 3 through the fourth openings.

[0056] To summarize, in the method of this invention, the requirement for the fourth dielectric layer to be "etchable" in a completely selective manner relative to the third dielectric layer 8 is also essential to the operability of the capacitors.

[0057] If this requirement is not met, during the step of forming the third openings 11 through the fourth dielectric layer (Figure 10), the third dielectric layer 8 would be destroyed or damaged, and thus compromising the operability of the capacitors C.

[0058] In standard processes, this feature imposes an additional burden on the integrated circuit manufacturing process. This feature is instead provided implicitly by the dual damascene interconnection scheme.

[0059] Advantageously, suitable materials for this fourth dielectric layer 10 are those having an organic base and being deposited by a spin-on method, both on account of this deposition technique being well established and compatible, and because they are etchable with an O_2-based chemistry which is selective in the respect of the etch stop layers 8 previously proposed.

[0060] Another characteristics that makes the use of such materials attractive is their low dielectric permittivity, which minimizes parasitic capacitances and interference between adjacent tracks and metal levels.

[0061] For the purpose, an appropriate choice of the thickness ratio between the fourth dielectric layer 10 and the third dielectric layer 8 can minimize the adverse effect on the interconnection by the high dielectric permittivity required of the last-mentioned layer.

Claims

1. A method for manufacturing capacitive elements integrated (C) on a semiconductor substrate (1), comprising at least the steps of:

   - forming a first dielectric layer (2) over said semiconductor substrate (1);
   - depositing a first metallization layer (3) on said first dielectric layer (2);
   - defining said first metallization layer (3) to provide lower plates (4) of capacitive elements and interconnection pads (5) in said dielectric layer (2);
   - forming a second dielectric layer (6) over said first dielectric layer; characterized in that it comprises the additional steps of:
   - forming first openings (7) aligned with said lower plates, through said second dielectric layer;
   - depositing a third dielectric layer (8) on said first dielectric layer and inside said first openings (7);
   - forming second openings (9) through said third dielectric layer aligned with said interconnection pads (5);
   - depositing a fourth dielectric layer (10) on the

whole wafer surface, said fourth dielectric layer (10) being "etchable" in a completely selective manner relative to said third dielectric layer (8);

- forming third openings (11) through said fourth dielectric layer aligned with said lower plates (4) as far down as the third dielectric layer (8);

- forming fourth openings (12) through said fourth dielectric layer (10), and the second dielectric layer (6) beneath, aligned with the second openings as far down as said pads (5);

- depositing a second metallization layer (13) and in said third (11) and fourth (12) openings, to respectively provide upper plates (13) for the capacitive elements (C) and complete interconnections (14) to the interconnection pads (5).

2. A method according to Claim 1, characterized in that the fourth dielectric layer (10) is made from the same material as said second dielectric layer (6).

3. A method according to Claim 1, characterized in that it comprises an additional step of planarizing said metallization layer.

4. A method according to Claim 2, characterized in that said fourth openings (12) are larger than said second openings (9).

5. A method according to Claim 2, characterized in that said third dielectric layer (8) is a conforming oxide.

6. A method according to Claim 5, characterized in that the third dielectric layer (8) is a tantalium or titanium oxide.

7. A method according to Claim 5, characterized in that the third dielectric layer (8) is a strontium or barium/strontium titanate.

8. A method according to either Claim 6 or 7, characterized in that the fourth dielectric layer (8) is made from an organic base material.

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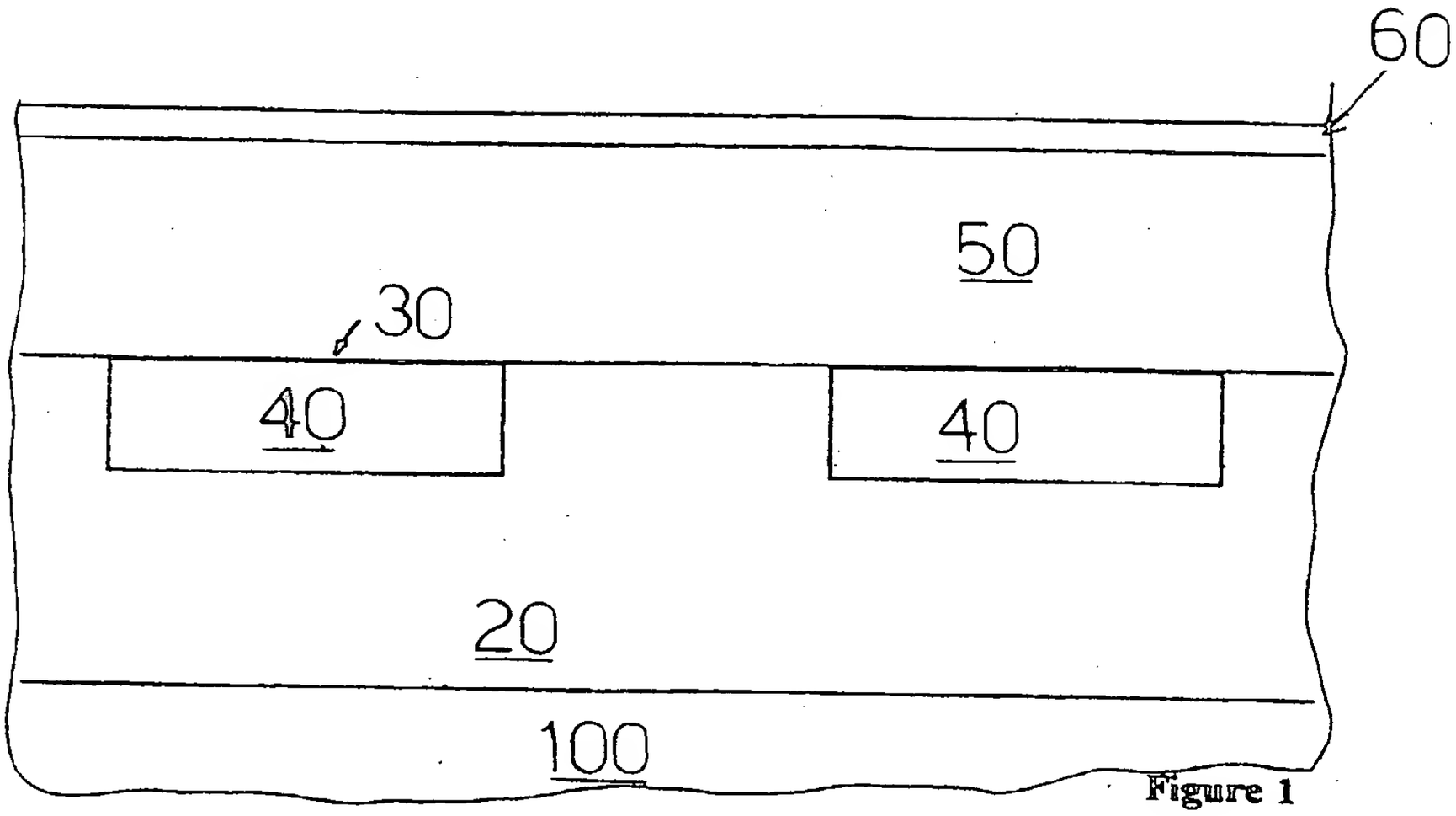

Figure 1

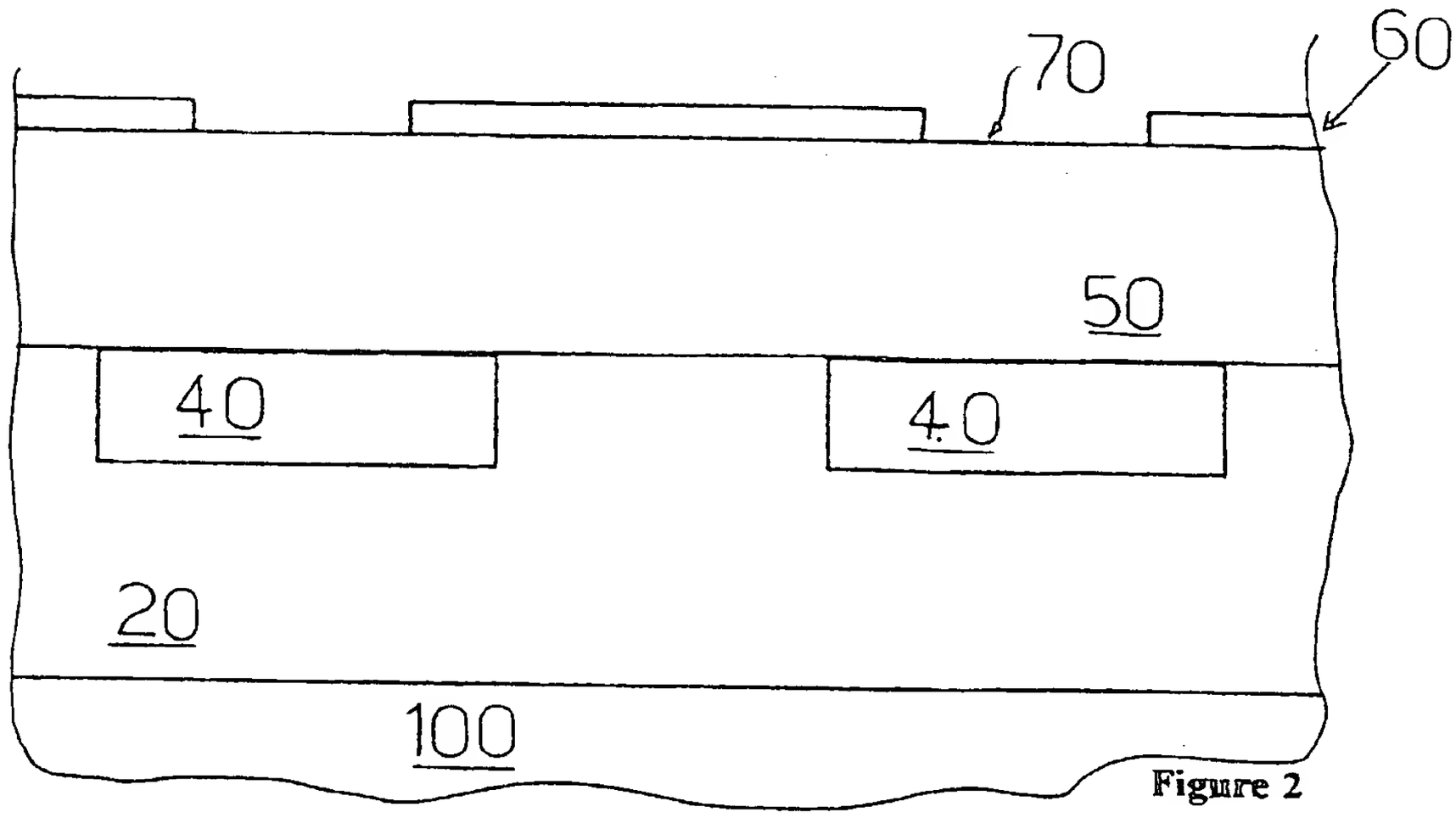

Figure 2

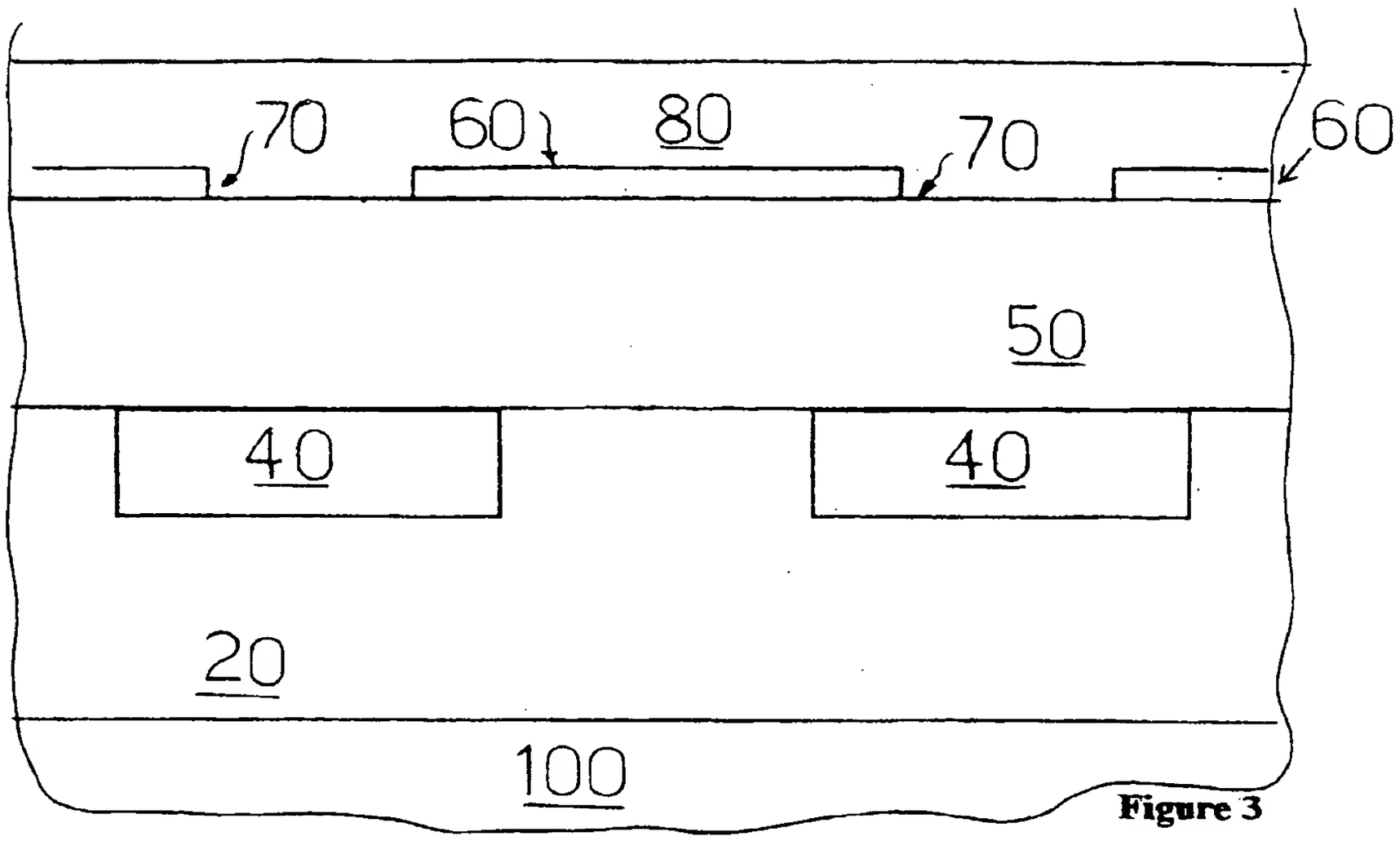

Figure 3

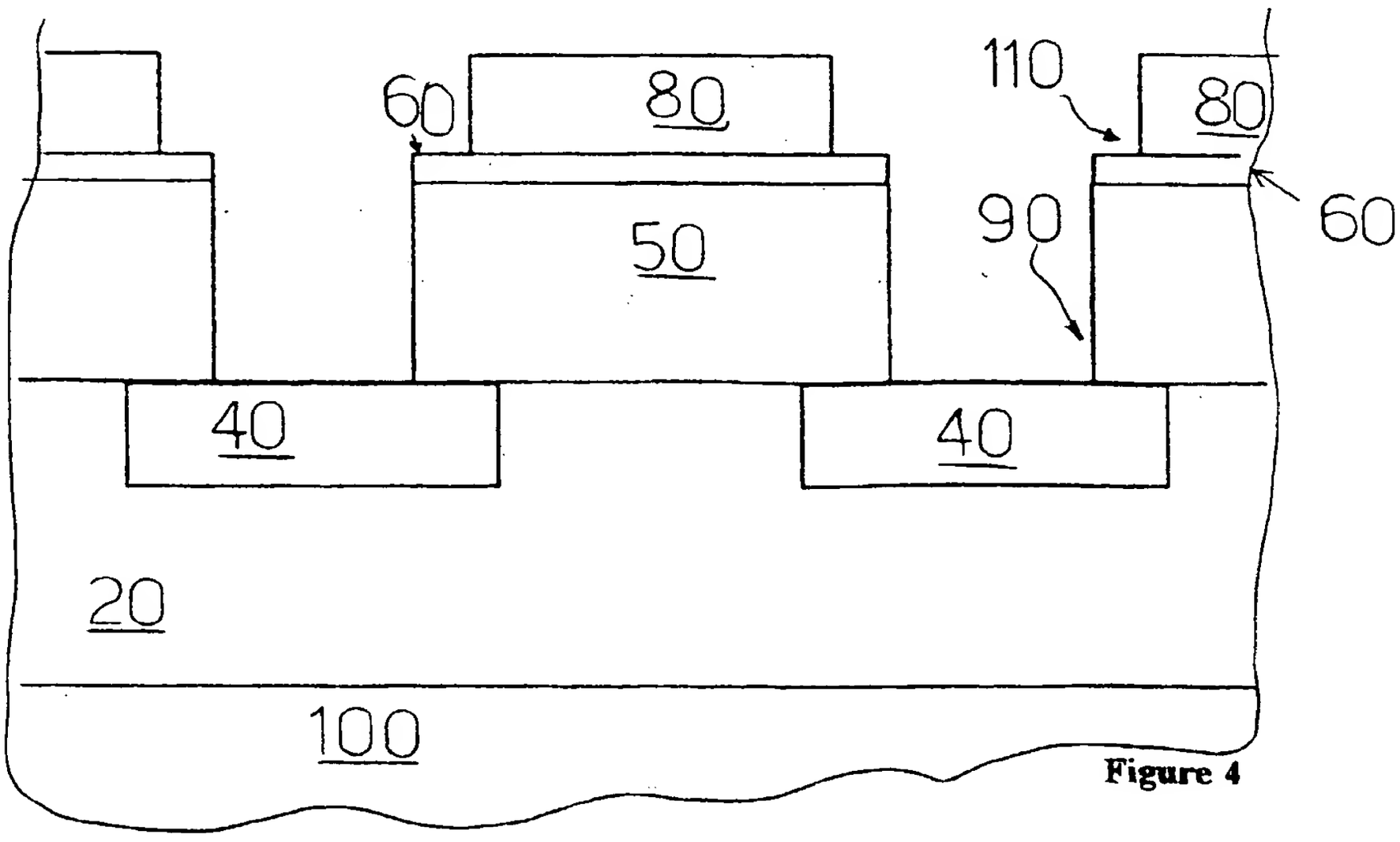

Figure 4

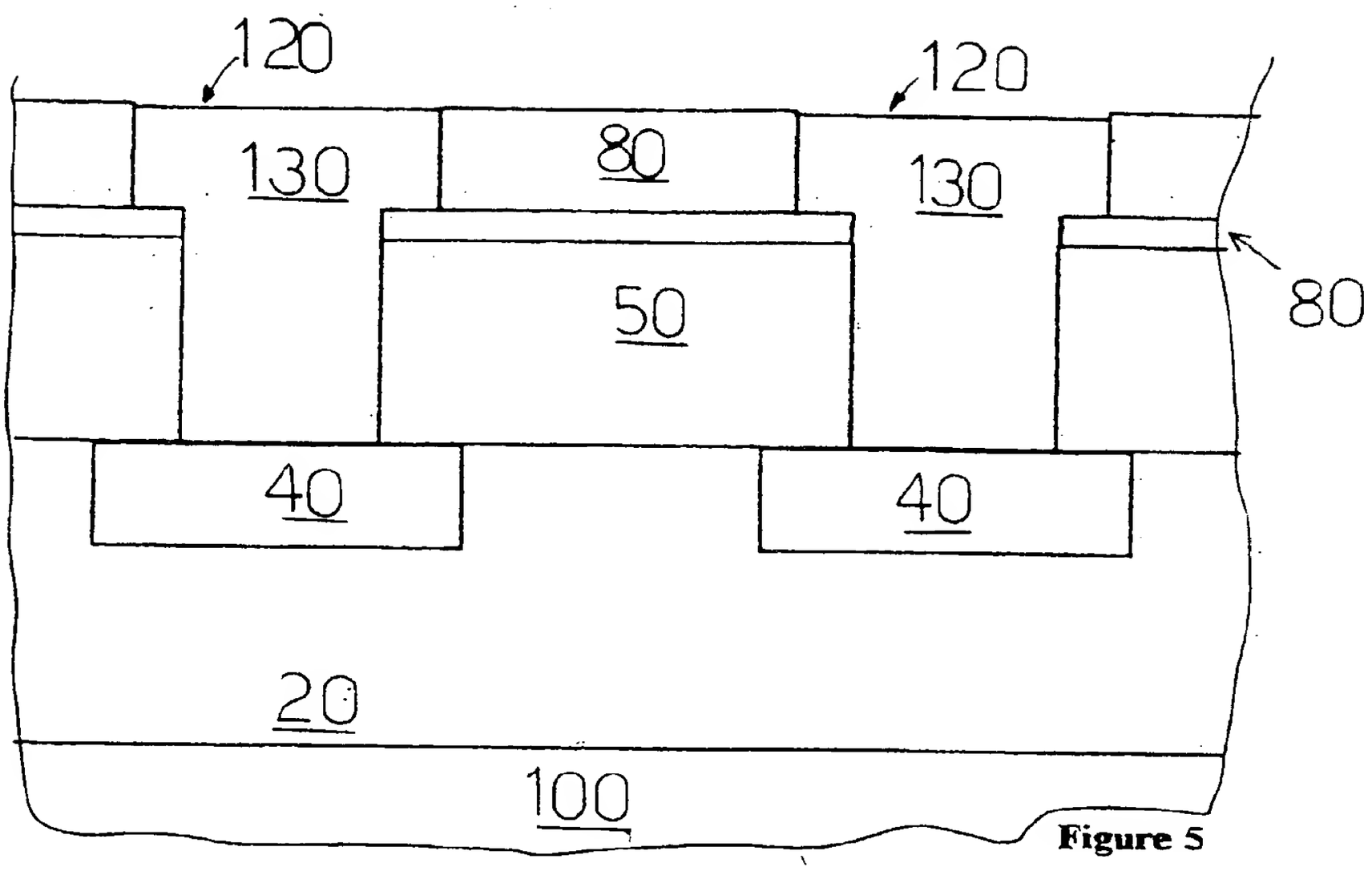

Figure 5

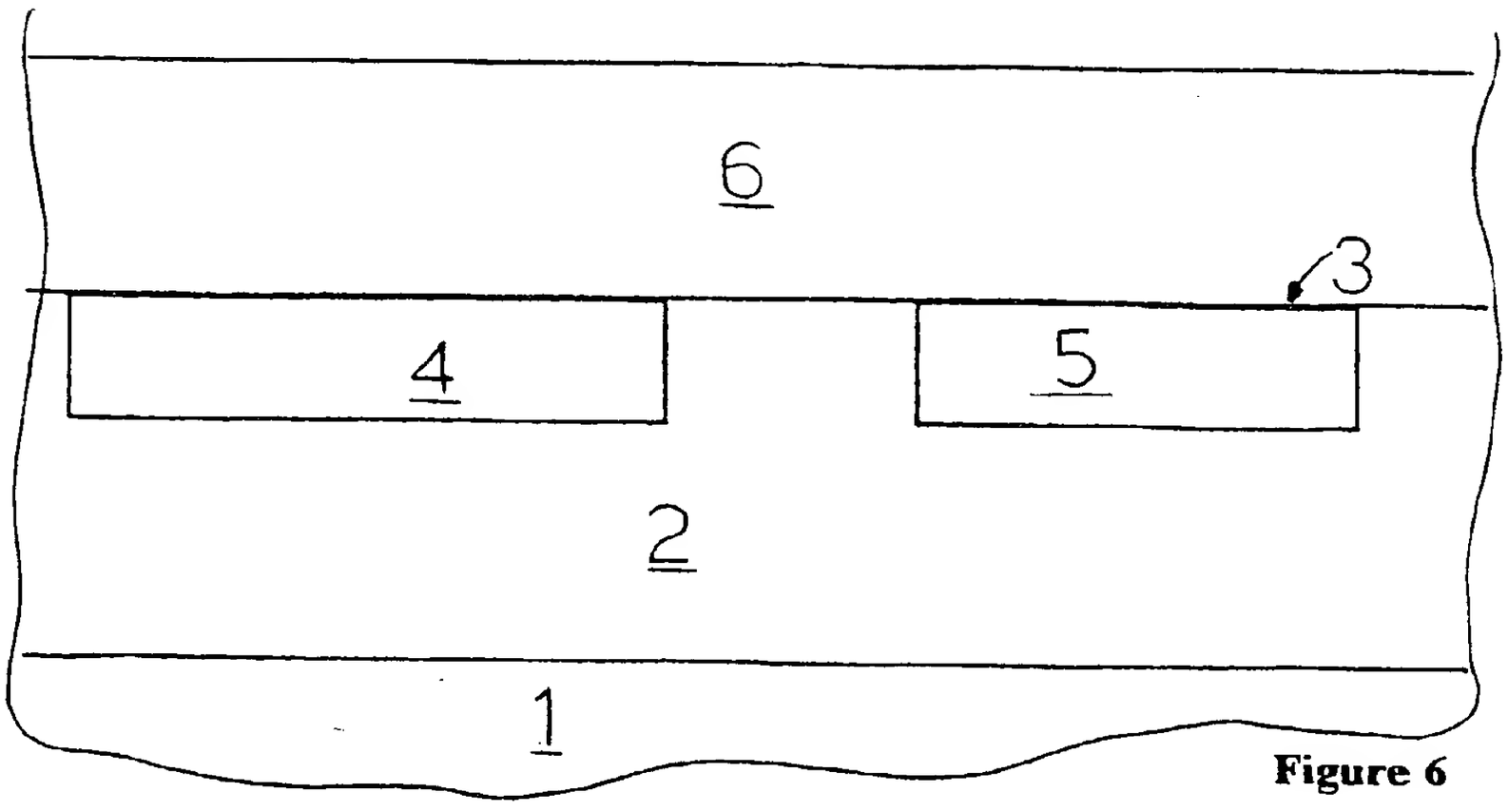

Figure 6

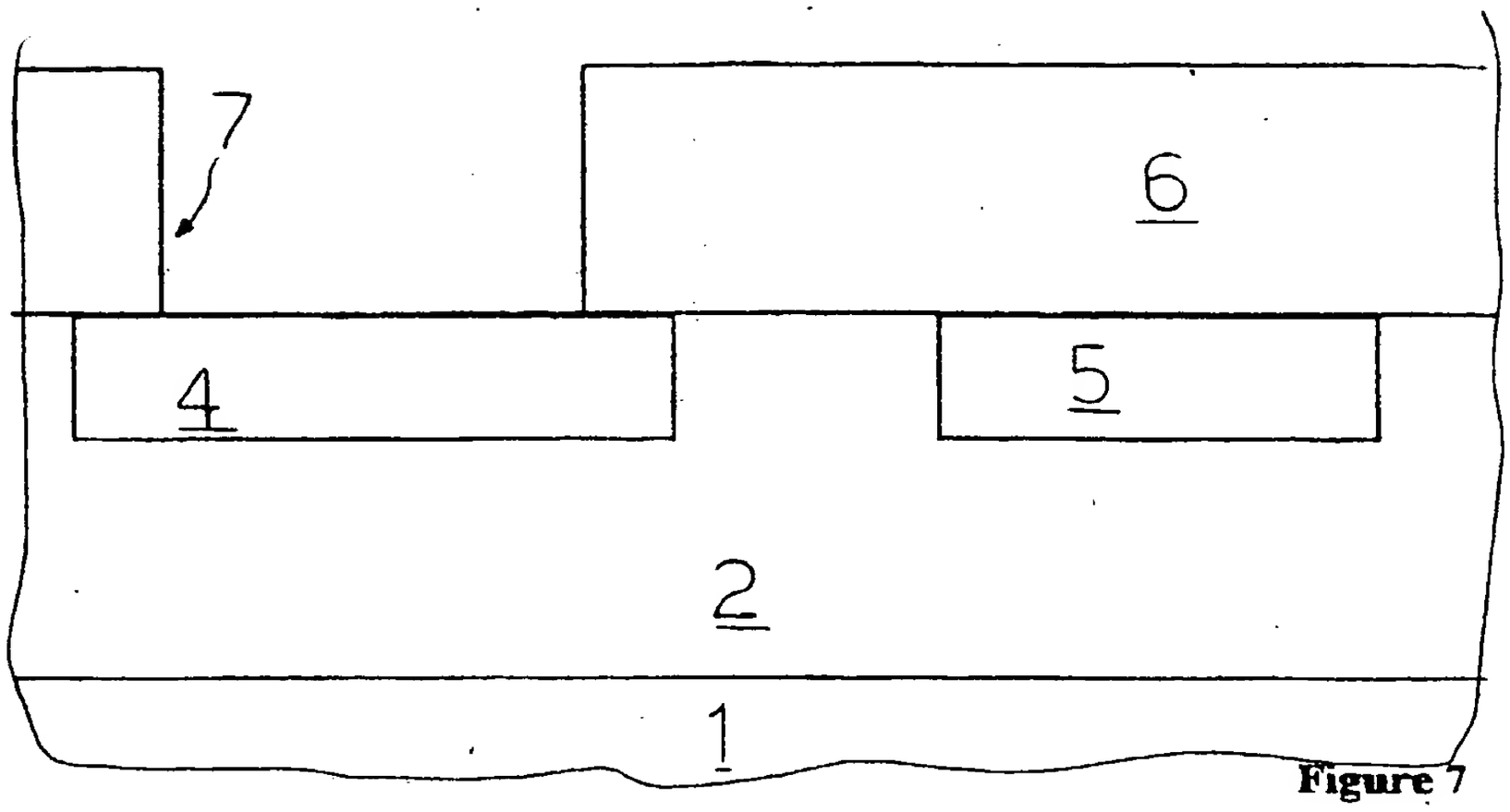

Figure 7

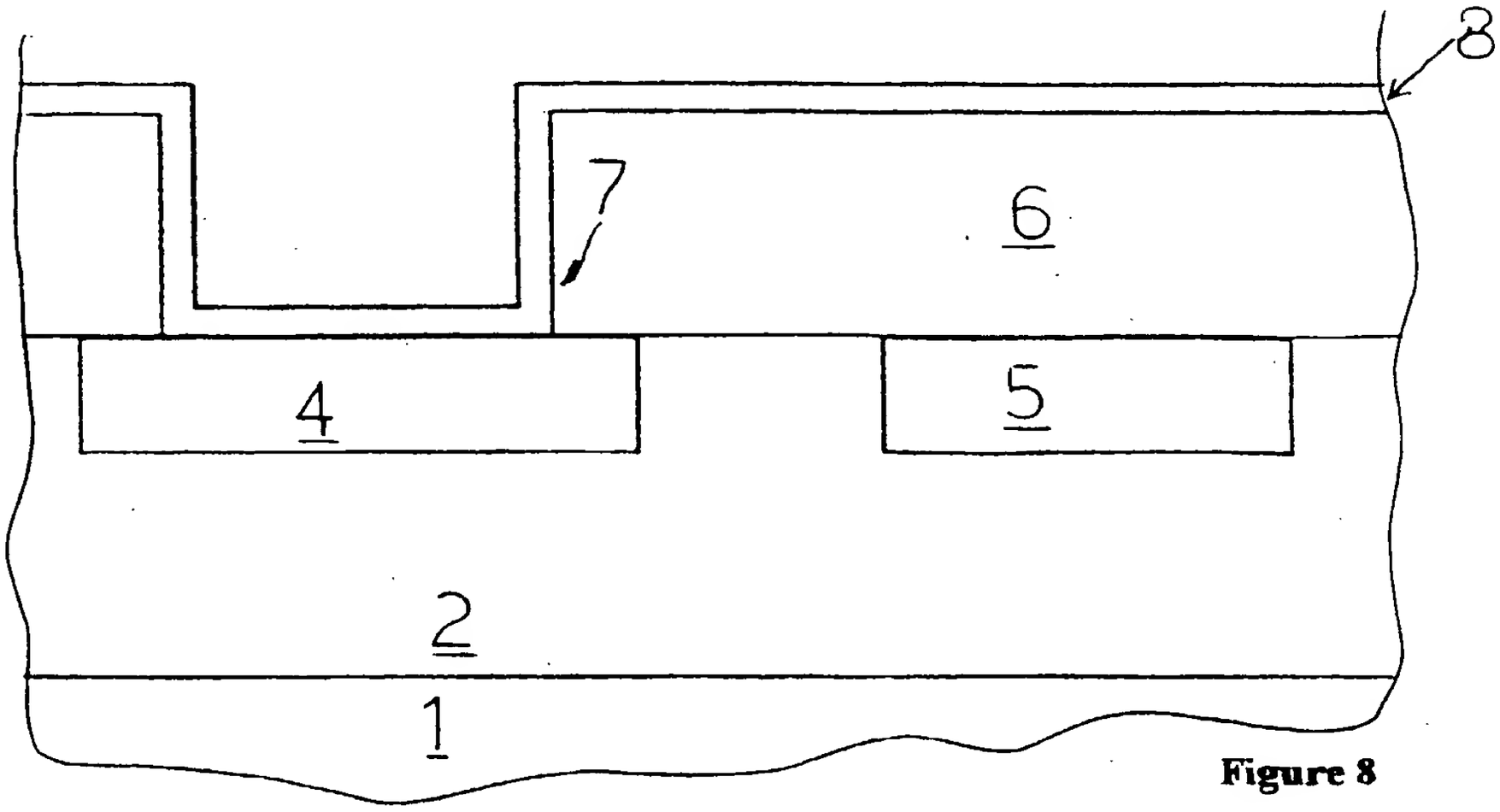

Figure 8

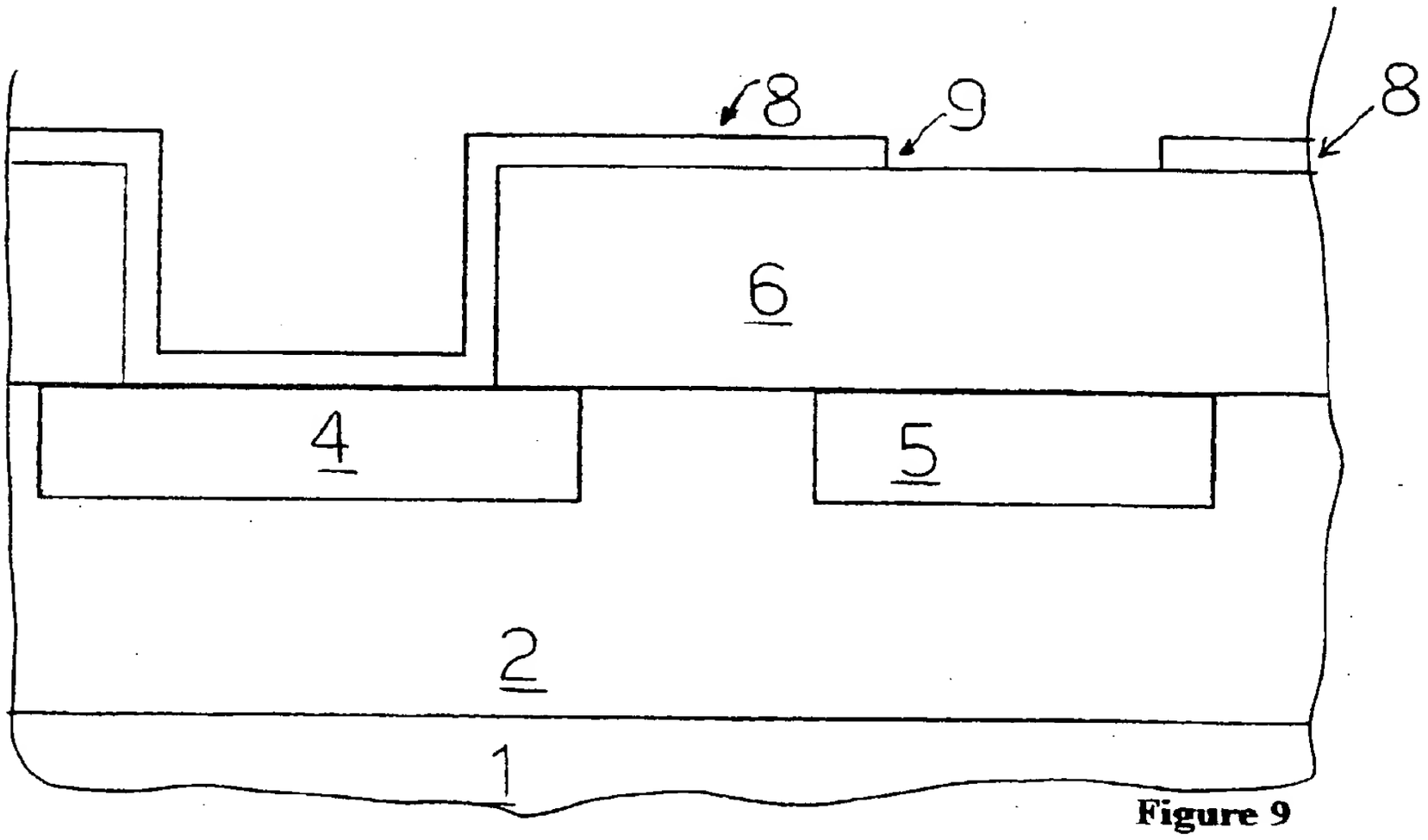

Figure 9

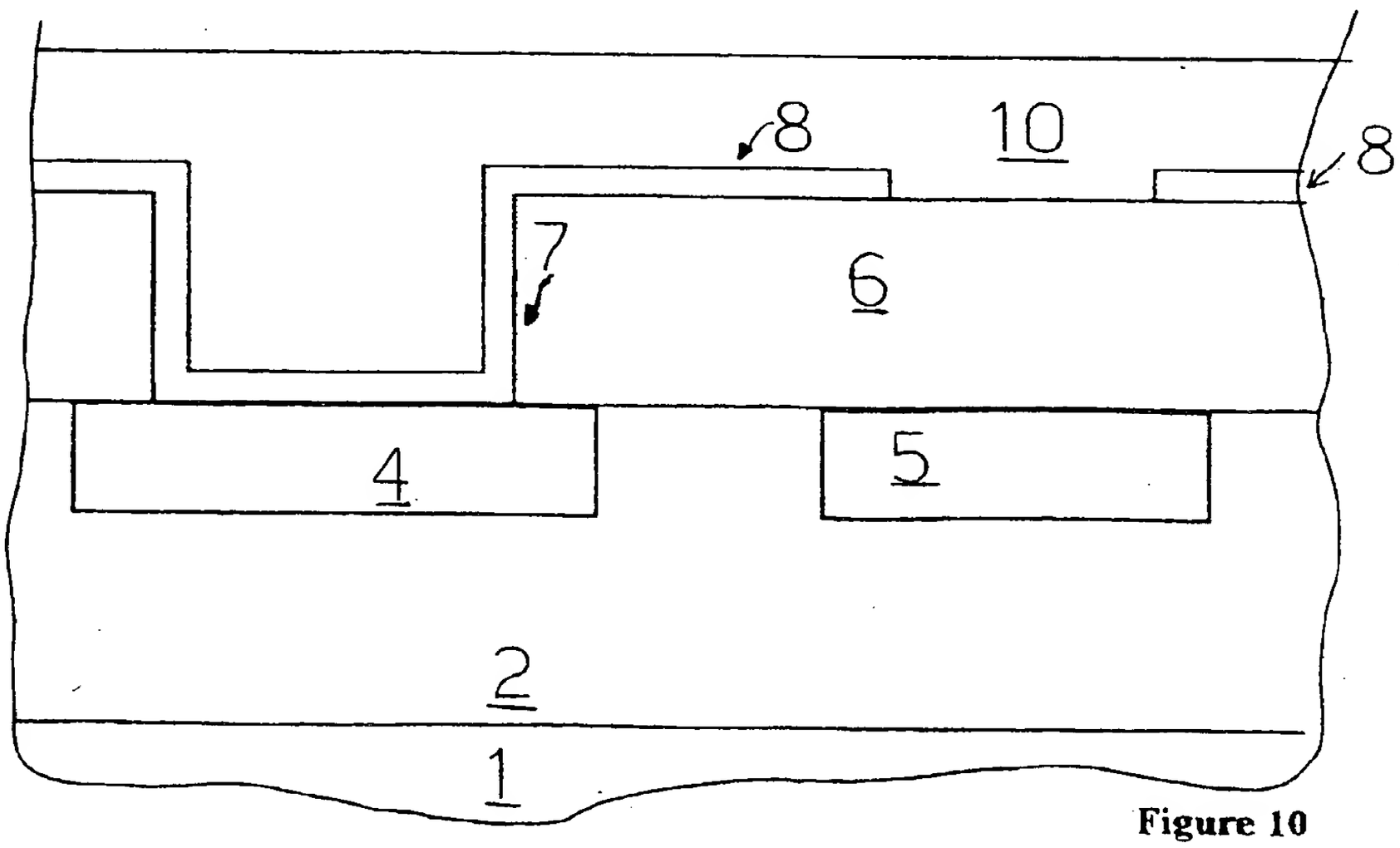

Figure 10

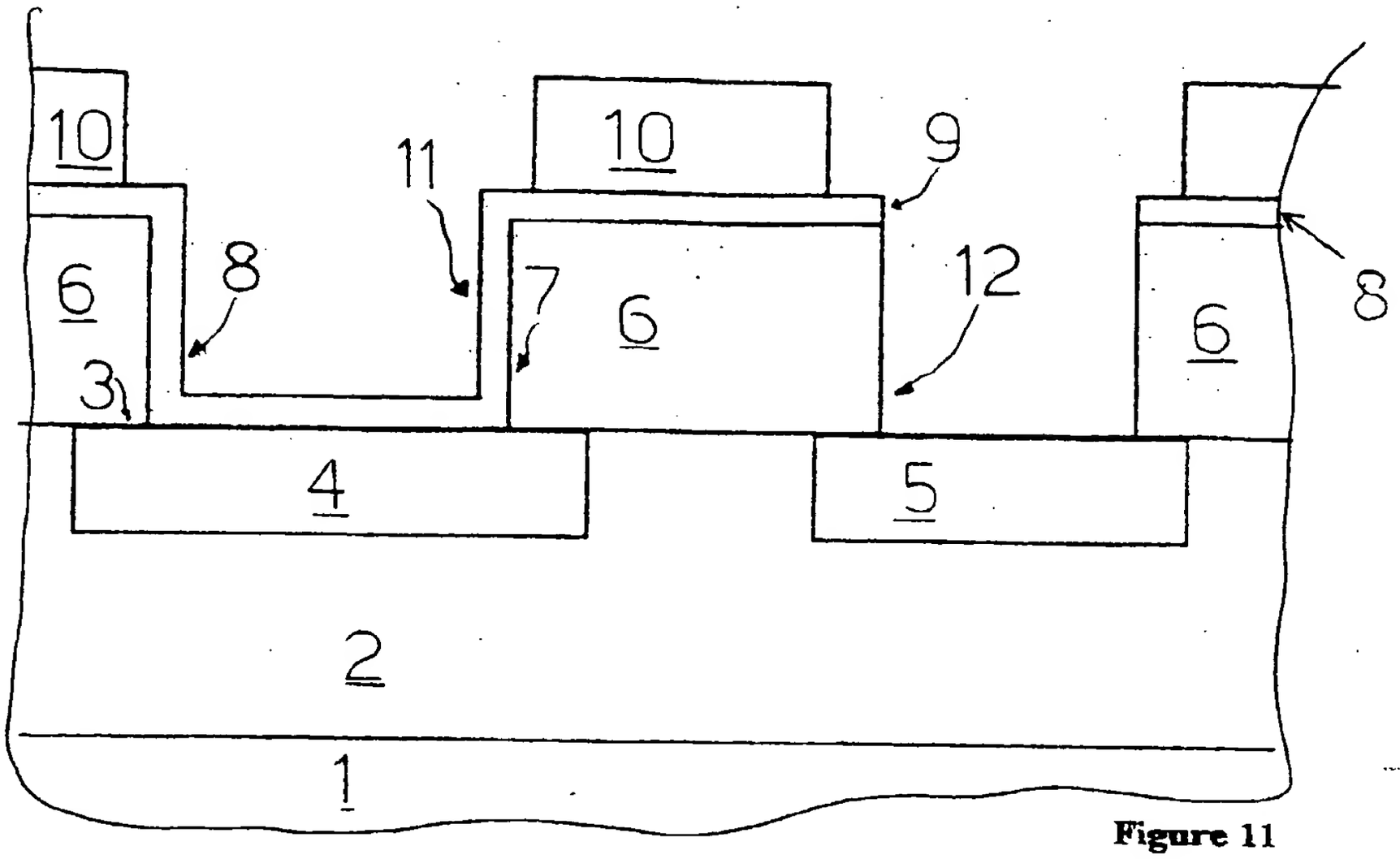

Figure 11

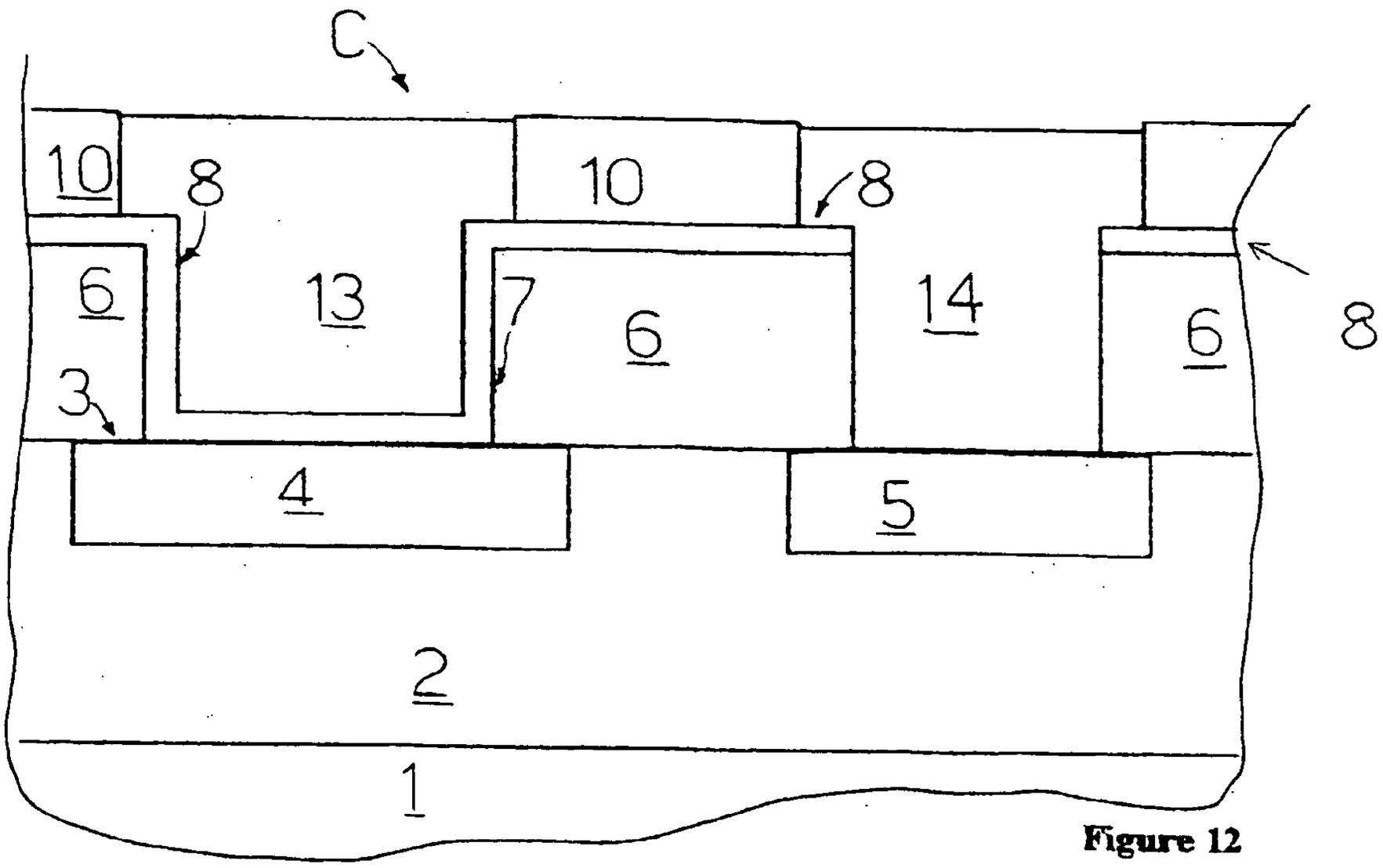

Figure 12

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0492

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 219 787 A (CAREY DAVID H ET AL) 15 June 1993 (1993-06-15) * figures 24-28 * * column 8, line 65 - column 9, line 45 *	1-8	H01L21/02 H01L21/768
A	EP 0 771 022 A (IBM) 2 May 1997 (1997-05-02) * figure 12 * * column 2, line 24 - column 4, line 19 *	1,3	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	15 December 1999	Le Meur, M-A

CATEGORY OF CITED DOCUMENTS

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15-12-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5219787 A	15-06-1993	US 5091339 A	25-02-1992
		US 5173442 A	22-12-1992
EP 0771022 A	02-05-1997	US 5708559 A	13-01-1998
		JP 9181258 A	11-07-1997

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